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EXAMINER	
TRAN, DENISE	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/470,329	BENNETT ET AL.	
	Examiner	Art Unit	
	Denise Tran	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/18/07.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 December 1999 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The applicant's amendment filed 6/18/07 has been considered. Claims 1-21 are presented for examination.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed limitations, claim 1, "retrying the first bus transaction and each subsequent non modifying bus transaction for the shared resource until the status bit is clear;" claim 3, "clearing the status bit randomly;" claim 4, "clearing the status bit at periodic intervals;" claim 5, "wherein the periodical intervals are longer than a length of time for a bus transaction to complete;" claim 6, " clearing the status bit using a pseudo-random method," and claims 7-9 have similar problems as discussed above, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The objection to the drawings is maintained. The applicant did not response to this objection.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-5 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert et al., U.S. Patent No. 6,041,376 (hereinafter Gilbert) in view of Arimilli et al., U.S. Patent No. 6,138,218 (hereinafter Arimilli).

As per claim 1, Gilbert shows a method of preventing live-lock in a multiprocessor system (e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

Identifying a first bus transaction that is a nonmodifying transaction on a shared resource (e.g. fig. 7, el. 76, col. 9, line 45-50);

identifying a second bus transaction that attempts to modify the shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

setting a status flag to indicate that a bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20); and

retrying the first bus transaction and each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared (e.g. fig. 8C, els. 114-118 and 122; and col. 11, lines 9-20 and col. 9, lines 14-18).

Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claim 7, Gilbert shows the use of a method of preventing live-lock in a multiprocessor system(e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

issuing a first bus transaction to read a cache line (e.g. fig. 7, el. 76, col. 7, lines 5-55 and col. 9, lines 48-52);

granting the cache line for the first bus transaction (e.g., col. 7, lines 5-55; col. 8, lines 5-10; fig. 8C, els. 118, 116, or 122)

issuing a second bus transaction that attempts to modify the cache line (fig. 6, el. 50; fig. 7, el. 76; and col. 7, lines 5-55 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the cache line (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a cache line; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

setting a status flag to indicate that a bus transaction attempting to modify the cache line is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20)

retrying the first bus transaction if the status flag is set (i.e., read request for the same cache line again when data being modify or invalid; e.g. fig. 8C, els. 114-116; col. col. 6, line 55 and et seq.; col. 4, line 40 to col. 5);

reissuing the second bus transaction that attempts to modify the cache line (e.g., fig. 8C, el. 120 and col. 11, lines 20);

granting the cache line for the reissued second bus transaction if the status flag is set for the cache line (e.g., fig. 8C, el. 122 and col. 11, lines 9-21).

Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claims 2 and 8, Gilbert teaches clearing the status flag when the reissued second bus transaction completes (e.g., fig. 8C, el. 122). As stated above, Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli col. 3, lines 1-3.

As per claim 4, Gilbert shows the use of clearing the status flag at periodic intervals (e.g., fig. 8C, el. 124). As stated above, Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claim 5, Gilbert shows the use of clearing the status flag at periodic intervals (e.g., fig. 8C, el. 124) and a given period of time can be any desired value (e.g., col. 11, lines 29-44). As stated above, Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Gilbert does not explicitly show periodical intervals being longer than a length of time for a bus transaction to complete. "Official Notice" is taken that both the concept and advantage of having periodical intervals being longer than a length of time for a bus transaction to complete are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the periodical intervals are longer than a length of time for a bus transaction to complete because it would allow sufficient time to finish the transaction and reduce the number of retry requests, thereby improving the system performance.

5. Claims 3, 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert et al., U.S. Patent No. 6,041,376, (hereinafter Gilbert) in view of Arimilli et al., U.S. Patent No. 6,138,218 (hereinafter Arimilli), as applied to claims 1 and 7 above, and further in view of Donley et al., U.S. Patent No. 5,761,446 (hereinafter Donley).

As per claims 3, 6, and 9, Gilbert shows the use of clearing the status flag by a counter where the counter can be any desired value (e.g., col. 11, lines 29-44). As stated above, Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and

allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo- random number (e.g., col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63.

6. Claims 10-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al., U.S. Patent No. 5,897,656, (hereinafter Vogt) in view of Gilbert et al., U.S. Patent No. 6,041,376) (hereinafter Gilbert).

As per claim 10, Vogt shows the use of a multiprocessor computer system comprising:

a plurality of processors (e.g., fig. 1, els. 112);

a resource shared by the plurality of processors (e.g., fig.1, el. 132);

at least one system bus interconnecting the shared resource and the plurality of processors (e.g., fig.1, el. 102);

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on the at least one system bus by one of the processors (e.g. figure 2, elements 208 and 210 and figure 5A, els 500 and fig. 6; and col. 25, line 54 to col. 26, line 27); and

a status indicator associated with each of the plurality of buffers (e.g. col. 26, lines 16-27; col. 28, lines 24-26), and nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the shared resource ((i.e., when the existing address for writing and the new address for reading; e.g., col. 25, lines 61-64; and col. 27, lines 32-45). Vogt does not specifically show the status indicator being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the shared resource and wherein the second bus transaction has priority over the first bus transaction to access the shared resource. Gilbert shows the use of a status indicator being set to indicate nonmodifying bus transactions is to be retried when a modifying bus transaction attempts to access the shared resource (e.g., fig. 8C, els. 110, 114, 116; col. 9, line 63-65 and col. 11, lines 9-20; and fig. 7, el. 76; col. 7, line 5 and col. 9, lines 48-52) and wherein the second bus transaction has priority over the first bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert col.2, lines 41-50.

As per claim 11, Vogt shows the use of four processors are coupled to each one of the system buses (e.g. figure 1, elements 112a-d and additional processors interpreted as at least four; and col. 16, lines 50-57).

As per claim 12, Vogt shows the use of at least one system bus comprises two processor buses (e.g. figure 1, elements 102 and 104).

As per claim 13, Vogt shows the use of four processors coupled to each one of the two processor buses (e.g. figure 1, elements 102, 104 and 112a-d and additional processors interpreted as at least four; and col. 16, lines 50-57.

As per claim 14, Vogt shows the use of an input/output bus (e.g. figure 1, element 106).

As per claim 15, Vogt shows the use of a multiple bus, multiprocessor computer system (e.g., fig. 1, els 102, 104, and 112) comprising:

a plurality of processors (fig. 1, els. 112);

a plurality of data cache memories (e.g. fig. 1, els. 114);

a system memory shared by the plurality of processors (e.g. fig. 1, el. 132);

at least two buses interconnecting the system memory with the plurality of data cache memories and the plurality of processors (e.g. fig. 1, els. 102 and 104); and

a controller (e.g. fig. 1, el. 130) comprising:

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on one of the buses by one of the processors (e.g. fig. 2, els. 208 and 210 and fig. 5A, els. 500 and fig. 6; and col. 25, line 54 to col. 26, line 27); and

a status indicator associated with each of the plurality of buffers (e.g. col. 26, lines 16-27; col. 28, lines 24-26), and nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the system memory ((i.e., when the existing address for writing and the new address for reading; e.g., col. 25, lines 61-64; and col. 27, lines 32-45). Vogt does not specifically show the status indicator being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the system memory and wherein the second bus transaction has priority over the first bus transaction to access the shared resource. Gilbert shows the use of a status indicator being set to indicate nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access a system memory (e.g., fig. 8C, els. 110, 114, 116; col. 9, line 63-65 and col. 11, lines 9-20; and fig. 7, el. 76; col. 7, line 5 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of processor requests for data by preventing other processors from

accessing data until the processor request is satisfied as taught by Gilbert col.2, lines 41-50.

As per claim 16, Vogt shows each one of the at least two buses is coupled to four of the processors (e.g. figure 1, elements 102, 104 and 112a-d and additional processors interpreted as at least four; and col. 16, lines 50-57).

As per claim 17, Vogt shows the use of an integrated circuit (e.g., fig. 2, el. 130 and col. 18, lines 43-46) comprising:

a bus interface to control a plurality of bus transactions (e.g. fig. 1, el. 204);

a coherency module to maintain cache coherency for a plurality of cache lines (e.g., fig. 2, el. 200); and

a buffer manager (e.g., fig. 2, el. 210) comprising,

a plurality of buffers (e.g. fig. 5A, els. 500), each one of the buffers to store information associated with one of the plurality of bus transactions received by the bus interface (e.g. fig. 5A, els. 500 and col. 26, lines 7-27); and

a plurality of status indicators where at least one of the status indicators associated with each of the buffers (e.g. fig. 5A, els. 502, 505), and nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the one of the cache lines (i.e., when the existing address for writing and the new address for reading; e.g., col. 25, lines 61-64; and col. 27, lines 32-45). Vogt does not specifically show the status indicator being set to indicate that nonmodifying bus

transactions are to be retried when a modifying bus transaction attempts to access the one of the cache lines and wherein the second bus transaction has priority over the first bus transaction to access the cache lines. Gilbert shows the use of a status indicator being set to indicate nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access a cache line (e.g., fig. 8C, els. 110, 114, 116; col. 9, line 63-65 and col. 11, lines 9-20; and fig. 7, el. 76; col. 7, line 5 and col. 9, lines 48-52); and wherein the second bus transaction has priority over the first bus transaction to access the cache lines (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert col.2, lines 41-50.

Vogt does not specifically show the status indicators indicating that one of the bus transactions attempting to modify one of the cache lines is retried. Gilbert shows the use of status indicators indicating that one of the bus transactions attempting to modify one of the cache lines is retried (e.g., fig. 8C, els. 110-122; col. 9, line 63-65 and col. 11, lines 9-24; and fig. 7, el. 76; col. 7, line 5 and col. 9, lines 48-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of

processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert col.2, lines 41-50.

As per claim 18, Vogt shows the use of the buffer manager further comprises logic to determine a type of bus transaction occurring on a bus (e.g. fig. 5A, el. 505 and col. 26, lines 24-27).

As per claim 19, Vogt shows the use of the buffer manager further comprises logic to determine if two of the bus transactions are contending for a same cache line (e.g. fig. 5B, els. 510 and col. 14, lines 10-30, col. 27, line 22 to col. 28, line 16).

As per claim 20, Vogt does not explicitly show logic to reset all of the plurality of status indicators. Gilbert shows logic to reset all of the plurality of status indicators (e.g., fig. 8C, els. 124 or 122; col. 2, lines 51-60; and col. 11, lines 9-30, where all the status flag can be reset at different times). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guarantee forward progress of processor requests for data by preventing other processors from accessing data until the processor request is satisfied and by limiting the amount of time that other processors are prevented from accessing the data as taught by Gilbert col. 2, line 41 to col. 3, line 8.

As per claim 21, Vogt shows the use of 64 buffers and 64 status indicators (e.g. figure 5A, els 500 and 502, 505 and col. 26, lines 15-20).

7. Applicant's arguments filed 6/18/07have been fully considered but they are not persuasive.

8. In the remarks, the applicant argued that neither Gilbert nor Arimilli teaches a feature "the second bus transaction has priority over the first bus transaction."

The examiner disagreed with the applicant's argument. The combination of Gilbert and Arimilli teaches the feature "the second bus transaction has priority over the first bus transaction." In particular, Gilbert shows

identifying a first bus transaction that is a nonmodifying transaction on a shared resource (e.g. fig. 7, el. 76, col. 9, line 45-50);

identifying a second bus transaction that attempts to modify the shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the

time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

9. In the remarks the applicant argued that Gilbert did not solve the live-lock problem as solved in the present application.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., solve the live-lock problem as solved in the present application) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In this case, the combination of Gilbert and Arimilli teaches what in the claim. Gilbert shows a method of preventing live-lock in a multiprocessor system (e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

Identifying a first bus transaction that is a nonmodifying transaction on a shared resource (e.g. fig. 7, el. 76, col. 9, line 45-50);

identifying a second bus transaction that attempts to modify the shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52), wherein the second bus

transaction has priority over the first bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

setting a status flag to indicate that a bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20); and

retrying the first bus transaction and each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared (e.g. fig. 8C, els. 114-118 and 122; and col. 11, lines 9-20 and col. 9, lines 14-18).

Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

10. In the remarks, the applicant argued that the status bit indicates that a bus transaction attempting to modify, whereas both Gilbert et al. and Arimili et al. disclose setting a status flag after the transaction already has the resource.

The examiner disagreed with the applicant's arguments because the combination of Gilbert et al. and Arimili et al. does not disclose setting a status flag after the transaction already has the resource as applicant alleged. For example, Gilbert, fig. 8C, els. 110 and 122 teaches the status flag being set before the transaction has the shared resource, e.g., the cache line. Also, it is noted that the claimed language "attempting to modify" does not exclude Gilbert et al. and Arimili et al. to set a status flag after the transaction already has the resource.

11. In the remarks, the applicant's argued that the cited references fails to teach "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending," claim 1.

The examiner disagreed with the applicant's arguments because the cited references teach "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending," claim 1. As stated in the rejections above, Gilbert shows a method of preventing live-lock in a multiprocessor system (e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

identifying a second bus transaction that attempts to modify a shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52);

setting a status flag to indicate that a bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20).

Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8,. lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

In further discussion, Gilbert, col. 2, lines 5-40 and fig. 8C, els. 110, 112, and 114; col. 9, lines 45-55 teaches a status (hold) flag being set to indicate a bus transaction attempting to modify a shared resource and allowing the modifying bus transaction to access the resource. Also, please see DECISION ON APPEAL mailed 7/11/06, page 8.

12. In the remarks, the applicant's argued that Arimilli fails to teach setting a status bit to indicate that a bus transaction attempting to modify the shared resource.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the combination of Gilbert and Arimilli shows the claimed limitation. In particular, As per claim 1, Gilbert shows a method of preventing live-lock in a multiprocessor system (e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

identifying a second bus transaction that attempts to modify the shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

setting a status flag to indicate that a bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20); and

retrying the first bus transaction and each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared (e.g. fig. 8C, els. 114-118 and 122; and col. 11, lines 9-20 and col. 9, lines 14-18).

Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert

because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Also, please see DECISION ON APPEAL mailed 7/11/06, page 8.

13. In the remarks, the applicant's argued that the cited references fail to teach setting a status bit to indicate that a bus transaction attempting to modify the cache line is pending or retrying the first bus transaction and each subsequent nonmodifying bus transaction for the shared resource until the status bit is clear.

The examiner disagreed with the applicant's arguments. Gilbert shows a method of preventing live-lock in a multiprocessor system (e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

Identifying a first bus transaction that is a nonmodifying transaction on the shared resource (e.g. fig. 7, el. 76, col. 9, line 45-50);

identifying a second bus transaction that attempts to modify a shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52);

identifying a second bus transaction that attempts to modify the shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying

bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

setting a status flag to indicate that a bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20); and

retrying the first bus transaction and each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared (e.g. fig. 8C, els. 114-118 and 122; and col. 11, lines 9-20 and col. 9, lines 14-18).

Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

14. In the remarks, the applicant's argued that Gilbert does not describe any system where a bus transaction which has been granted a resource may be force to retry as an incoming bus transaction steps and sets a status flag to keep claim the resource or the

cache line or the combination of the cited references does not describe all the elements of claim 7.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., system where a bus transaction which has been granted a resource may be force to retry as an incoming bus transaction steps and sets a status flag to keep claim the resource or the cache line) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The combination of Gilbert and Arimilli teaches what in the claim and Gilbert shows the use of a method of preventing live-lock in a multiprocessor system(e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

issuing a first bus transaction to read a cache line (e.g. fig. 7, el. 76, col. 7, lines 5-55 and col. 9, lines 48-52);

granting the cache line for the first bus transaction (e.g., col. 7, lines 5-55; col. 8, lines 5-10)

issuing a second bus transaction that attempts to modify the cache line (fig. 6, el. 50; fig. 7, el. 76; and col. 7, lines 5-55 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the cache line (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a cache line; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

setting a status flag to indicate that a bus transaction attempting to modify the cache line is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20)

retrying the first bus transaction if the status flag is set (i.e., read request for the same cache line again when data being modify or invalid; e.g. fig. 8C, els. 114-116; col. col. 6, line 55 and et seq.; col. 4, line 40 to col. 5);

reissuing the second bus transaction that attempts to modify the cache line (e.g., fig. 8C, el. 120 and col. 11, lines 20);

granting the cache line for the reissued second bus transaction if the status flag is set for the cache line (e.g., fig. 8C, el. 122 and col. 11, lines 9-21).

Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

15. In the remarks, the applicant's argued that the combination of Gilbert, Arimili, and Donley did not teach all the limitations of claims 3,6, and 9.

The examiner disagreed with the applicant's arguments because the combination of Gilbert, Arimili, and Donley teaches all the claimed limitations as stated in the rejections of claims 3, 6, and 9 above. Also, please see DECISION ON APPEAL mailed 7/11/06, pages 8 and 10.

16. In the remarks, the applicant's argued that the cited references, Vogt and Gilbert did not teach all the limitations of claims 10, 15, or 17.

The examiner disagreed with the applicant's arguments because the combination of Vogt and Gilbert references teaches all the claimed limitations as stated in the rejections of claims 10, 15, or 17 above. Also, please see DECISION ON APPEAL mailed 7/11/06, pages 10-12.

17. In the remarks, the applicant's argued that the Office Action fails to state a prima facie case of obviousness with respect to claims 2, 4-5, and 9.

The examiner disagreed with the applicant's arguments. As stated in the rejections above with respect to claims 1, 7, 2, 4-5, and 9, and the examiner's answers to the applicant's arguments with respect to claims 1 and 7 above, the combination of Gilbert and Arimilli teaches all the limitations of claims 1, 7, 2, 4-5, and 9. Therefore, the Office Action established a prima facie case of obviousness with respect to claims 2, 4-5, and 9. Also, please see DECISION ON APPEAL mailed 7/11/06, pages 8 and 10.

18. In the remarks, the applicant's argued that the Office Action fails to state a prima facie case of obviousness with respect to claims 11-14, 16, and 18-21.

The examiner disagreed with the applicant's arguments. As stated in the rejections above with respect to claims 10, 15, 17, 11-14, 16, and 18-21, and the examiner's answers to the applicant's arguments with respect to claims 10, 15, 17 above, the combination of Gilbert and Arimilli teaches all the limitations of claims 10, 15, 17, 11-14, 16, and 18-21. Therefore, the Office Action established a prima facie case of obviousness with respect to claims 2, 4-5, and 9. Also, please see DECISION ON APPEAL mailed 7/11/06, pages 10-12.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and Friday from 8:30 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Denise Tran

9/3/07